J-Link-OB-STM32F072-128KB (Cortex-M)

User guide of the onboard debug probe based on STM32F072Cx MCU

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Manual versions

This manual describes the current version. If you find an error in the manual, please report it to us and we will try to assist you as soon as possible.

Contact us for further information on topics that are not yet documented.

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Manual version	Revision	Date	By	Description
0.00	1	171012	NG	Initial Version

About this document

Assumptions

This document assumes that you already have a solid knowledge of the following:

- The software tools used for building your application (assembler, linker, C compiler).
- The C programming language.
- The target processor.
- DOS command line.

If you feel that your knowledge of C is not sufficient, we recommend *The C Programming Language* by Kernighan and Richie (ISBN 0–13–1103628), which describes the standard in C programming and, in newer editions, also covers the ANSI C standard.

How to use this manual

This manual explains all the functions and macros that the product offers. It assumes you have a working knowledge of the C language. Knowledge of assembly programming is not required.

Typographic conventions for syntax

This manual uses the following typographic conventions:

Style	Used for
Body	Body text.
`Keyword`	Text that you enter at the command prompt or that appears on the display (that is system functions, file- or pathnames).
`Parameter`	Parameters in API functions.
`Sample`	Sample code in program examples.
`Sample comment`	Comments in program examples.
Reference	Reference to chapters, sections, tables and figures or other documents.
GUIElement	Buttons, dialog boxes, menu names, menu commands.
Emphasis	Very important sections.

Table of contents

Chapter 1

Why J-Link OB?

The J-Link on-board (J-Link OB) was designed in order to provide a low-cost, space-saving and on-board alternative to the general J-Link, for eval board manufacturers. J-Link OB can be used with the same software package as the general J-Links and can be used with the same utilities (as far as the feature set of the J-Link OB supports this)

> **Note**
>
> It is not allowed to use J-Link-OB-STM32F072-128KB (Cortex-M) for stand-alone emulators.

Chapter 2

Supported target CPU cores

For a list of cores supported by this J-Link OB model, please refer to here:
J-Link OB Model overview

Chapter 3

Supported target interfaces

The J-Link-OB-STM32F072-128KB (Cortex-M) supports the following target interfaces:

- SWD (+ SWO)

It may only be used with Cortex-M target CPUs.

3.1 Target interface pins

The J-Link-OB-STM32F072-128KB (Cortex-M) provides the following target interface signals:

- #RESET (PA1 / Pin 11)
- SWCLK (PA2 / Pin 12)
- SWO (PA3 / Pin 13)
- SWDIO (PA4 / Pin 14)
- TXD (PA9 / Pin 30)
- RXD (PA10 / Pin 31)
- CTS (PA7 / Pin 17)
- RTS (PA6 / Pin 16)

Which signals are required depends on what features shall be supported on the evaluation board. If support for a specific feature or interface is not required, the spare pins should be left open. For more information about which target interface requires which signals, please refer to the following sections.

3.2 Target interface SWD

If SWD (+ optional SWO) support is required on the target hardware to be designed, the following signals need to be connected:

- #RESET (PA1 / Pin 11)
- SWCLK (PA2 / Pin 12)
- SWO (PA3 / Pin 13)
- SWDIO (PA4 / Pin 14)

If SWO support is not required (e.g. when the target CPU is Cortex-M0/M0+ based, which does not provide SWO support), the SWO signal can be left open.

3.3 Target interface VCOM

This J-Link OB model can support virtual COM port (VCOM) as an optional and additional target interface. For more information about what VCOM is, please refer to *J-Link VCOM functionality* .
If VCOM (+ optional hardware flow control) support is required on the target hardware to be designed, the following signals need to be connected:

- TXD (PA9 / Pin 30)
- RXD (PA10 / Pin 31)
- CTS (PA7 / Pin 17)
- RTS (PA6 / Pin 16)

If hardware flow control support is not required, the CTS and RTS signal can be left open.

Chapter 4

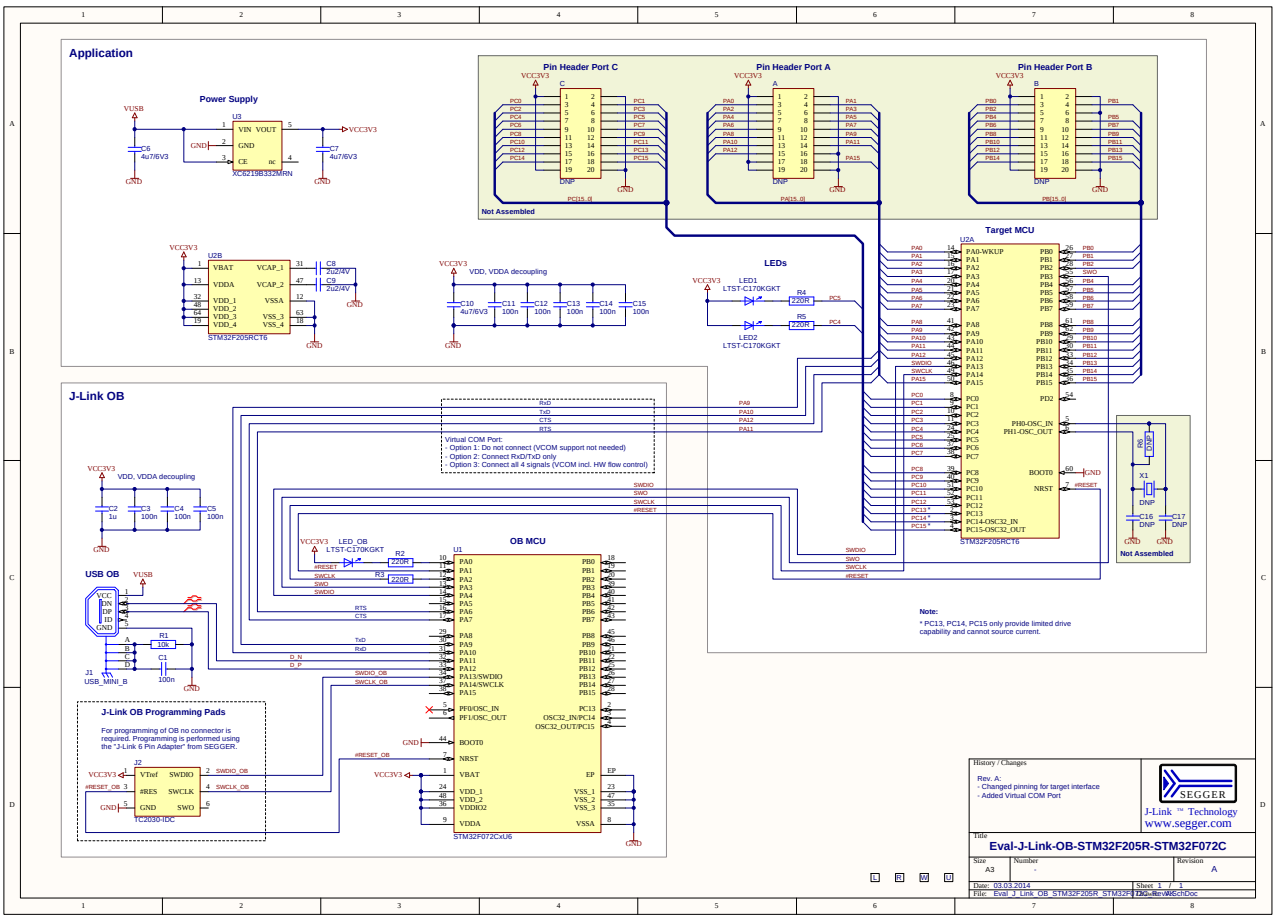
Compatible MCUs as J-Link OB host

The J-Link-OB-STM32F072-128KB (Cortex-M) is based on the ST STM32 F072C 48 MHz, 128 KB flash, 16 KB RAM series MCUs. The following microcontrollers are compatible to this J-Link OB model:

- ST STM32F072CB LQFP 48
- ST STM32F072CB UFQFPN 48
- ST STM32F072CB WLCSP 49L
- ST STM32F072RB LQFP 64
- ST STM32F072RB UFBGA 64L
- ST STM32F072VB LQFP 100
- ST STM32F072VB UFBGA 100

Chapter 5

Schematics



Chapter 6

Glossary

This chapter describes important terms used throughout this manual.

Adaptive clocking

A technique in which J-Link / J-Trace sends out a clock signal and waits for the returned clock from the target device before generating the next clock pulse. The technique allows the J-Link / J-Trace interface unit to adapt to different signal drive capabilities, different cable lengths and variable target clock speeds. Adaptive clocking can be used when it is supported by the connected target device.

RESET

Abbreviation of System Reset. The electronic signal which causes the target system other than the TAP controller to be reset. This signal is also known as "nSRST" "nSYSRST", "nRST", or "nRESET" in some other manuals. See also nTRST.

nTRST

Abbreviation of TAP Reset. The electronic signal that causes the target system TAP controller to be reset. This signal is known as nICERST in some other manuals. See also nSRST.

RTCK

Returned TCK. The signal which allows Adaptive Clocking.

TCK

The electronic clock signal which times data on the TAP data lines TMS, TDI, and TDO.

TDI

The electronic signal input to a TAP controller from the data source (upstream). Usually, the TDI signal of J-Link is connected to the TDI of the first TAP controller in a JTAG chain.

TDO

The electronic signal output from a TAP controller to the data sink (downstream). Usually, the TDO signal of J-Link is connected to the TDO of the last TAP controller in a JTAG chain.

TMS

The electronic signal Test Mode Select is an input to the TAP controller and it is used to select different stages of state machine. It is clocked in into the TAP controller using the TCK signal.(upstream). Usually, the TMS output signal of J-Link is connected to the TMS input of the first TAP controller in a JTAG chain. For Cortex-M CPUs this signal may also be used as the bidirectional data signal SWDIO when the CPU is accessed in serial wire debug mode SWD.

SWD

A serial communication protocol for Cortex M CPUs which may used for communication with a debug device as an alternative communication channel to JTAG. The SWD communication uses less pins.

SWDIO

The bidirectional electronic signal for communication of a Cortex M CPU accessed in serial wire debug mode. Normally, the TMS input pin of the Cortex M CPU is used as SWDIO pin in serial wire mode.

SWCLK

The electronic signal which times data on the SWDIO data line used in serial wire debug mode. The SWCLK pin is typically the TCK pin used as JTAG clock input, when JTAG is also supported by the device.

SWO

The electronic asynchronous signal for trace data output or SWV output data which may be sent by the application on a Cortex-M CPU running in serial wire debug mode. J-Link-OB-STM32F072-128KB (Cortex-M) is able to receive the data in asynchronous mode when SWO of the target CPU is connected to the SWOin signal of J-Link-OB-STM32F072-128KB (Cortex-M). Normally the SWO output signal of a Cortex-M CPU is directed via the TDO signal pin, but may be separated on some devices.